Pattern Stream & Capture  
Requirements

Version 0.1

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## Public Version History

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| --- | --- | --- | --- |
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# Introduction

This block is generic block that is integrated into FPGA that behaves as Tester for various ASICs. The FPGA in general is responsible of driving functional or scan pattern to the ASIC & check the pattern it gets back. This block, as part of the whole FPGA is responsible on the streaming & capturing of the pattern.

Refer to next figure



Figure ‎2‑1: Stream & Capture as part of FPGA

# Requirements

## High Level

Refer to the next figure:



Figure ‎3‑1: Stream & Capture signals

* Clock – 100Mhz. All signals besides the parameters are synchronous to it.
* Reset – Asynchronous reset, active low

There are 2 mode of operation:

1. Captured pattern is saved to memory, Stream & Capture block doesn’t check the pattern. In this mode, the Read port is used to get the Stream Pattern & the Write port is used to send to the memory the Captured pattern
2. Captured pattern isn’t saved to memory, but it’s checked by the Stream & Capture block to expected pattern. In this mode, the Read port is used to get both Stream & Captured patterns. The Write port is used to send info on the failures if any (i.e. in what capture cycles the pattern check failed)

Upon “go” the Stream & Capture block should read pattern from the FPGA memory & stream it towards the ASIC. In parallel, it should capture the pattern that it gets back from the ASIC.

It’s recommended to use internal FIFOs to handle the handshake towards the FPGA memory.

When the configured size ends (all pattern was streamed), the Stream & Capture block should provide “Finish” indication together with the pattern check status (in operation mode B)

## Debug

* Stream & Capture block should use internal ILA with test probes as required for debug support
* Stream & Capture block should support mode in which known (generated internally) pattern is streamed